ABSTRACT OF THE DISCLOSURE

A system and method for implementing a CPU/Network Device Interface that reduces the CPU involvement in managing the interface. New data structures in shared memory that are either read-only or write-only by CPU allow the CPU to efficiently utilize techniques such as write-posting and cache prefetching. Additionally, hardware-assisted packet transmission and high-level packet flow control reduce the burden on the CPU. A fair allocation system assures fair access to the receive interface by multiple line cards.